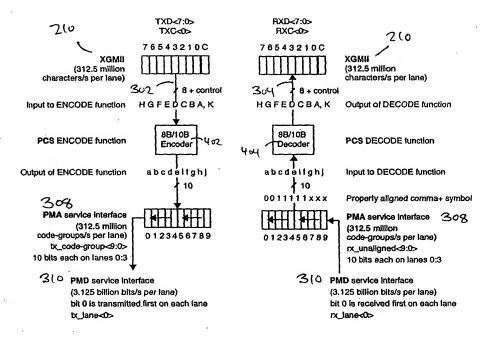


F16.3

Lane 0 only shown



F16.4

XGMII TXC	XGMII TXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal data transmission
1	07	K28.0 or K28.3 or K28.5	Idle in IIII
1.	07 ·	K28.5	Idle in ITII
1	9C	K28.4	Sequence
1	FB	K27.7	Start
Į.	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Other value in Table 36-2	See Table 36-2	Reserved XGMII character
1	Any other value	K30.7	Invalid XGMII character
NOTE-V	alues in TXD colum	n are in hexadecimal.	

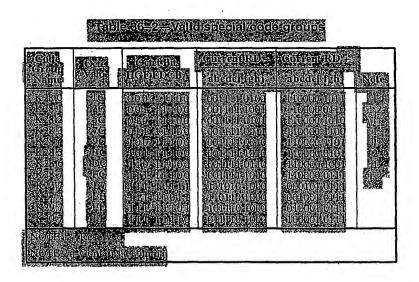


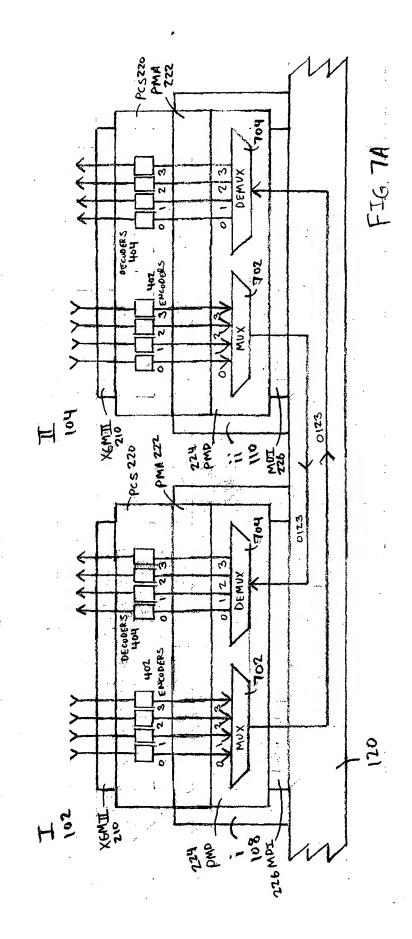
FIG.5

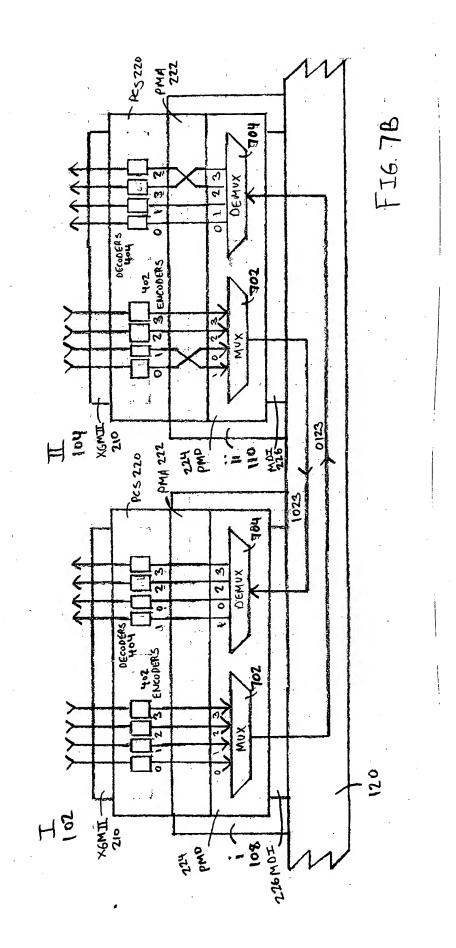
Code	Ordered_Set	Number of code-groups	Encoding
HIH	Idle		Substitute for XGMII Idle
IIKII	Sync column	4	/K28.5/K28.5/K28.5/K28.5/
IIRI)	Skip column	4	/K28.0/K28.0/K28.0/K28.0/
liAli	Align column	4	/K28.3/K28.3/K28.3/
	Encapsulation		
IISII	Start column	4	/K27.7/Dx.y/Dx.y/Dx.y/ ^a
liTi	Terminate column	4	Terminate code-group in any lane
llT ₀ ll	Terminate in Lane 0	4	/K29.7/K28.5/K28.5/K28.5/
llT ₁ ii	Terminate in Lane 1	4	/Dx.y/K29.7/K28.5/K28.5/ ^a
llT ₂ ll	Terminate in Lane 2	4	/Dx.y/Dx.y/K29.7/K28.5/ ^a
llT3	Terminate in Lane 3	4	/Dx.y/Dx.y/Dx.y/K29.7/ ^a
	Control		
/E/	Error code-group	1	/K30.7/
	Link Status		
IIQII	Sequence ordered_set	4	/K28.4/Dx.y/Dx.y/Dx.y/ ^a
IILFII	Local Fault signal	4	/K28.4/D0.0/D0.0/D1.0/
liRFII	Remote Fault signal	4	/K28.4/D0.0/D0.0/D2.0/
llQrsvdll	Reserved	4	! LF and ! RF
	Reserved		
llFsigll	Signal ordered_set	4	/K28.2/Dx.y/Dx.y/Dx.y/ ^{a,b}

"/Dx.y/ indicates any data code-group

^bReserved for INCITS T11.

FIG. 6





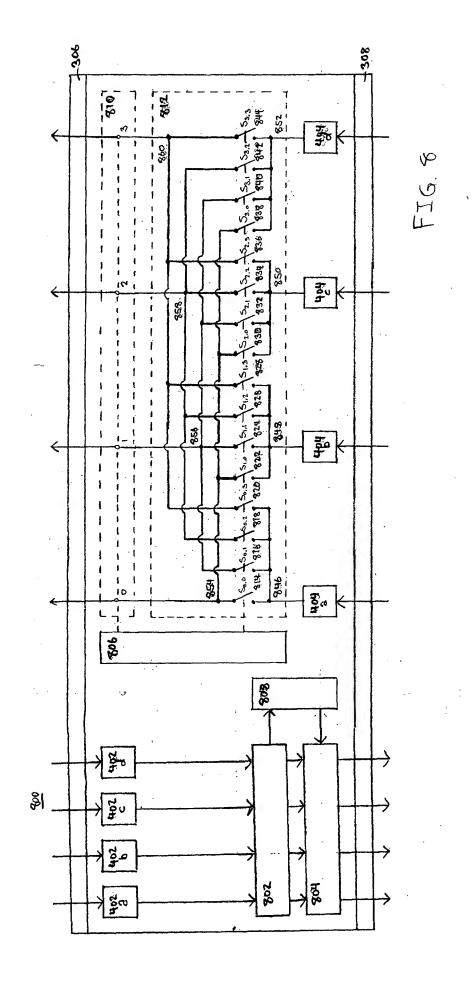
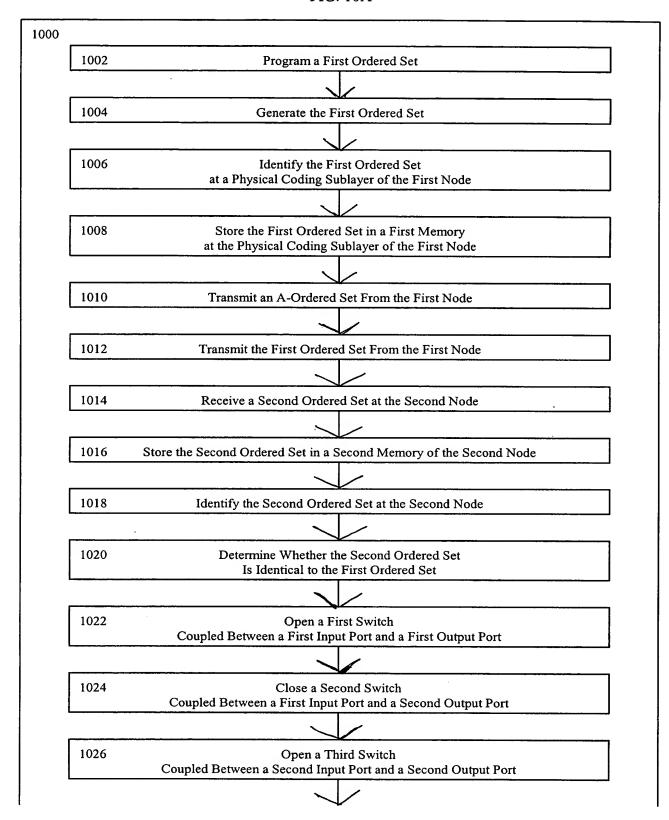


FIG. 9

Received Special Ordered Set	Lane Correction Switch Configuration
/Da.b/Dc.d/De.f/Dg.h/	/S _{0.0} /S _{1.1} /S _{2.2} /S _{3.3} /
/Da.b/Dc.d/Dg.h/De.f/	/S _{0.0} /S _{1.1} /S _{2.3} /S _{3.2} /
/Da.b/De.f/Dc.d/Dg.h/	/S _{0.0} /S _{1.2} /S _{2.1} /S _{3.3} /
/Da.b/De.f/Dg.h/Dc.d/	/S _{0.0} /S _{1.2} /S _{2.3} /S _{3.1} /
/Da.b/Dg.h/Dc.d/De.f/	/S _{0.0} /S _{1.3} /S _{2.1} /S _{3.2} /
/Da.b/Dg.h/De.f/Dc.d/	/S _{0.0} /S _{1.3} /S _{2.2} /S _{3.1} /
/Dc.d/Da.b/De.f/Dg.h/	/S _{0.1} /S _{1.0} /S _{2.2} /S _{3.3} /
/Dc.d/Da.b/Dg.h/De.f/	/S _{0.1} /S _{1.0} /S _{2.3} /S _{3.2} /
/Dc.d/De.f/Da.b/Dg.h/	/S _{0.1} /S _{1.2} /S _{2.0} /S _{3.3} /
/Dc.d/De.f/Dg.h/Da.b/	/S _{0.1} /S _{1.2} /S _{2.3} /S _{3.0} /
/Dc.d/Dg.h/Da.b/De.f/	/S _{0.1} /S _{1.3} /S _{2.0} /S _{3.2} /
/Dc.d/Dg.h/De.f/Da.b/	/S _{0.1} /S _{1.3} /S _{2.2} /S _{3.0} /
/De.f/Da.b/Dc.d/Dg.h/	/S _{0.2} /S _{1.0} /S _{2.1} /S _{3.3} /
/De.f/Da.b/Dg.h/Dc.d/	/S _{0.2} /S _{1.0} /S _{2.3} /S _{3.1} /
/De.f/Dc.d/Da.b/Dg.h/	/S _{0.2} /S _{1.1} /S _{2.0} /S _{3.3} /
/De.f/Dc.d/Dg.h/Da.b/	/S _{0.2} /S _{1.1} /S _{2.3} /S _{3.0} /
/De.f/Dg.h/Da.b/Dc.d/	/S _{0.2} /S _{1.3} /S _{2.0} /S _{3.1} /
/De.f/Dg.h/Dc.d/Da.b/	/S _{0.2} /S _{1.3} /S _{2.1} /S _{3.0} /
/Dg.h/Da.b/Dc.d/De.f/	/S _{0.3} /S _{1.0} /S _{2.1} /S _{3.2} /
/Dg.h/Da.b/De.f/Dc.d/	/S _{0.3} /S _{1.0} /S _{2.2} /S _{3.1} /
/Dg.h/Dc.d/Da.b/De.f/	/S _{0.3} /S _{1.1} /S _{2.0} /S _{3.2} /
/Dg.h/Dc.d/De.f/Da.b/	/S _{0.3} /S _{1.1} /S _{2.2} /S _{3.0} /
/Dg.h/De.f/Da.b/Dc.d/	/S _{0.3} /S _{1.2} /S _{2.0} /S _{3.1} /
/Dg.h/De.f/Dc.d/Da.b/	/S _{0.3} /S _{1.2} /S _{2.1} /S _{3.0} /



1028 Close a Fourth Switch
Coupled Between a Second Input Port and a First Output Port

FIG. 11

